REMARKS

In the non-final Office Action, the Examiner rejected claims 42-67 under the judicially created doctrine of obviousness-type double patenting as unpatentable over claims 1 and 16 of U.S. Patent Application, Serial No. 09/534,838; rejected claims 1-8, 22, 23, and 26-28 under 35 U.S.C. § 102(e) as anticipated by Sindhu et al. (U.S. Patent No. 5,905,725); rejected claim 24 under 35 U.S.C. § 103(a) as unpatentable over Sindhu et al.; and rejected claims 9 and 29 under 35 U.S.C. § 103(a) as unpatentable over Sindhu et al. in view of Sandquist (U.S. Patent No. 5,506,841). The Examiner objected to claims 10-21, 25, and 30-41 as dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten in independent form to include all of the features of the base claim and any intervening claims.

By this Amendment, Applicants amend claim 1 to improve form. Applicants also submit herewith a terminal disclaimer. Applicants appreciate the Examiner's identification of allowable subject matter, but respectfully traverse the Examiner's rejections under 35 U.S.C. §§ 102 and 103. Claims 1-82 remain pending.

Initially, in a prior Restriction Requirement, dated April 23, 2004, the Examiner required restriction under 35 U.S.C. § 121 to either Group I, claims 1-72, allegedly drawn to load balancing packet processing, or Group II, claims 73-82, allegedly drawn to time scheduling for transmission of packets. Applicants elected claims 1-72 with traverse and presented arguments why the restriction was improper.

M.P.E.P. § 821.01 states:

> Where the initial requirement is traversed, it should be reconsidered. If, upon reconsideration, the examiner is still of the opinion that restriction is proper, it should be

> repeated and made final in the next Office action. (See MPEP § 803.01.) In doing so, the examiner should reply to the reasons or arguments advanced by applicant in the traverse.

The Examiner did not address Applicants' arguments presented in the traverse. Further, the Examiner did not make the restriction final. In fact, the Examiner did not mention the restriction or claims 73-82. Applicants continue to submit that the restriction was improper and request clarification as to the status of claims 73-82.

In paragraph I of the Office Action, the Examiner rejected claims 42-67 under the judicially created doctrine of obviousness-type double patenting as unpatentable over claims 1 and 16 of U.S. Patent Application, Serial No. 09/534,838. Applicants assume that the Examiner intended the rejection to be a provisional rejection since Patent Application Serial No. 09/534,838 is still pending.

Applicants submit herewith a Terminal Disclaimer to obviate the provisional double patenting rejection over pending Patent Application Serial No. 09/534,838. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 42-67 and their timely allowance.

In paragraph II of the Office Action, the Examiner rejected claims 1-8, 22, 23, and 26-28 under 35 U.S.C. § 102(e) as allegedly anticipated by Sindhu et al. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as

complete detail as contained in the claim. See M.P.E.P. § 2131. Sindhu et al. does not disclose or suggest the combination of features recited in claims 1-8, 22, 23, and 26-28.

Amended claim 1, for example, recites a combination of features of a network device comprising at least one sprayer configured to receive packets on at least one incoming packet stream and distribute the packets according to a load balancing scheme, a plurality of packet processors connected to the at least one sprayer and configured to receive the packets from the at least one sprayer and process the packets to determine routing information for the packets, and at least one desprayer configured to receive the processed packets from the packet processors and transmit the packets on at least one outgoing packet stream.

Sindhu et al. does not disclose or suggest the combination of features recited in claim 1. For example, Sindhu et al. does not disclose or suggest a plurality of packet processors connected to the at least one sprayer and configured to receive the packets from the at least one sprayer and process the packets to determine routing information for the packets.

The Examiner alleged that Sindhu et al. discloses these features and cited Figure 5A (items 514, 515, 510, and 505), column 2, lines 14-67, and column 5, lines 26-53 of Sindhu et al. for support (Office Action, page 3). Applicants disagree.

In Figure 5A, Sindhu et al. illustrates input switch 100. The Examiner identified input switch 100 and input ports 107 as allegedly corresponding to the at least one sprayer recited in claim 1 (Office Action, page 3). Therefore, the contents of input switch 100, namely items 514, 515, 510, and 505, cannot also be equivalent to a plurality of packet processors that connect to the at least one sprayer to receive packets from the at least one sprayer, as required by claim 1.

Further, Sindhu et al. discloses that item 514 corresponds to a key reading engine, item 515 corresponds to a linking engine, item 510 corresponds to an indirect cell processor, and item 505 corresponds to an output processor. Nowhere does Sindhu et al. disclose or suggest that any of these items processes packets received from at least one sprayer to determine routing information for the packets, as required by claim 1.

At column 2, lines 14-67, Sindhu et al. discloses:

> In general, in one aspect, the invention provides a router for switching a data packet between a source and destination in a network including a plurality of input ports each including a data handler. The data handler divides a data packet into one or more fixed length cells. The router includes a plurality of output ports at least one of which is for routing the data packet to the destination and a memory divided into a plurality of memory banks. A input switch receives fixed length cells from the input ports and writes a single cell in a cell slot time span to each memory bank. An output switch routes cells received from the memory to an appropriate output port.
>
> Aspects of the invention include the following features. The input switch includes a linking engine for linking cells in the data packet to allow retrieval of the data packet from non-contiguous locations in the memory. The router further includes an indirect cell generator for generating one or more indirect cells. The linking engine tracks the location in the memory where consecutive cells of the data packet are stored and provides an address in memory of each cell in the data packet for storage in indirect cells.
>
> The input switch time division multiplexes the writing of data packets to the memory such that consecutive cells from the input port are written to consecutive banks in the memory. The input switch includes a key reading engine for extracting key information from a first cell received at the input switch associated with the data packet. The router further includes a controller coupled to the input switch for receiving the key information therefrom. The controller decodes destination information from the key information received from the input switch and outputs a notification defining a routing of the data packet from the memory to the output port.
>
> The output port includes a result processor for receiving the notification from the controller and initiates a transfer of the data packet from the memory to the output port. The input switch includes a reservation table for scheduling transfers from the memory to the output switch. The output switch routes the notification to the output port and thereafter the output port issues a request to the input switch to transfer the data packet from memory to the output port through the output switch. The request from the output port is stored in the reservation table. The requests to transfer cells from memory to the output switch are time domain multiplexed so that during one cell slot time span at most a single read request is issued to each bank in the memory for servicing. The memory outputs at most a single cell per bank in one cell slot time span.

> One advantage of the invention is that packets may be switched through the router at line rates without requiring the storage of the packets in expensive high speed memory by providing a switching architecture that efficiently manages and routes packets through the switch.

Nothing in this section, or any other section of Sindhu et al., discloses or suggests a plurality of packet processors connected to at least one sprayer and configured to receive packets from the at least one sprayer and process the packets to determine routing information for the packets, as recited in claim 1.

At column 5, lines 26-53, Sindhu et al. discloses:

> Referring to FIG. 5a, input switch 100 includes a round robin data handler 500, one or more input port interfaces (501-0 through 501-7, one for each input port 107), one or more memory interfaces 502 (502-0 through 502-7, one associated with each memory bank), a like plurality of pointers 504 (504-0 through 504-7), an output processor 505, one or more output port interfaces 506 (506-0 through 506-7, one for each output port 108), a reservation table 508, an indirect cell processor 510, controller interface 512 and read controller 516.
>
> Round robin data handler 500 receives cells from each input port and transfers them to output processor 505 for output to an appropriate memory bank 105 in memory 104. Round robin data handler 500 services the inputs (cells) received on input port interfaces 501 in a round robin, time division multiplexed manner. That is, for a given cell slot, one cell from each input port is received at the round robin data handler 500 and subsequently transferred to output processor 505 for transfer at the next cell slot to a memory bank 105 in memory 104. At the next time cell slot, data handler 500 transfers the next cell received from the same input port to output processor 505 for transfer to a different memory bank. In one embodiment, the next cell received is transferred to the next memory bank (next in numerical order) in the memory array. Alternatively, another time dependent permutation may be used to control the transfer of successive cells from the same input port.

This section of Sindhu et al. refers to operations performed by input switch 100, which the Examiner alleged was equivalent to the at least one sprayer recited in claim 1. Nowhere in this section, or elsewhere, does Sindhu et al. disclose or suggest a plurality of packet processors connected to the at least one sprayer and configured to receive packets from the at

least one sprayer and process the packets to determine routing information for the packets, as recited in claim 1.

For at least these reasons, Applicants submit that claim 1 is not anticipated by Sindhu et al. Claims 2-8, 22, and 23 depend from claim 1 and are, therefore, not anticipated by Sindhu et al. for at least the reasons given with regard to claim 1. Claims 2-8, 22, and 23 also recite additional features not disclosed or suggested by Sindhu et al.

For example, claim 2 recites that the at least one sprayer includes a plurality of sprayers, where each of the sprayers is connected to distribute packets to each of the packet processors according to the load balancing scheme. Sindhu et al. does not disclose or suggest the combination of features recited in claim 2.

The Examiner alleged that Sindhu et al. discloses these features and cited Figures 2B (items 107 and 100) and 5B, column 4, lines 21-51, column 2, lines 14-67, and column 5, lines 26-53 (Office Action, page 4). Applicants disagree.

As explained above, Sindhu et al. does not disclose or suggest a plurality of packet processors. Therefore, Sindhu et al. cannot disclose or suggest a plurality of sprayers, where each of the sprayers is connected to distribute packets to each of the packet processors according to a load balancing scheme, as recited in claim 2. None of the portions of Sindhu et al. identified by the Examiner disclose or suggest these features.

The Examiner referred to the round robin procedure of Sindhu et al. as allegedly being equivalent to the load balancing scheme recited in claim 2. Applicants disagree. At column 5, lines 37-53 (recreated above), Sindhu et al. discloses that the round robin procedure is used by round robin data handler 500 when servicing input cells received on input port interfaces

501. Sindhu et al. discloses that for a given cell slot, one cell from each input port is received at round robin data handler 500 and subsequently transferred to output processor 505 for transfer at the next cell slot to a memory bank 105 in memory 104. Nowhere does Sindhu et al. disclose or suggest that each of input ports 107 and input switch 100 (which the Examiner alleged was equivalent to a plurality of sprayers) is connected to distribute packets to each of key reading engine 514, linking engine 515, indirect cell processor 510, and output processor 505 (which the Examiner alleged was equivalent to the packet processors) according to the round robin procedure (which the Examiner alleged was the equivalent to the load balancing scheme), as would be required by claim 2.

For at least these additional reasons, Applicants submit that claim 2 is not anticipated by Sindhu et al.

Claim 3 recites that the at least one sprayer includes at least one receive interface configured to receive the packets from the at least one incoming packet stream, a shared memory configured to store the packets received by the at least one receive interface, and a plurality of transmit interfaces configured to transmit the packets stored in the shared memory to the packet processors. Sindhu et al. does not disclose or suggest the combination of features recited in claim 3.

The Examiner alleged that Sindhu et al. discloses these features and cited items 107 and 100 as allegedly equivalent to the at least one receive interface, items 514, 515, 510, and 505 as allegedly equivalent to the shared memory, and items 102 and 108 as allegedly equivalent to the plurality of transmit interfaces (Office Action, page 4). Applicants disagree.

Applicants note that claim 3 recites features included in the at least one sprayer and the Examiner identified the same items that the Examiner identified as allegedly being equivalent to the at least one sprayer, the plurality of packet processors, and the at least one desprayer recited in claim 1. Applicants submit that the Examiner's confusing identification of items in Sindhu et al. falls short of establishing a proper case of anticipation with regard to claim 3.

Further, the items identified by the Examiner cannot be equated to the features recited in claim 3. For example, Sindhu et al. does not disclose or suggest that any of key reading engine 514, linking engine 515, indirect cell processor 510, and output processor 505 is a shared memory.

For at least these additional reasons, Applicants submit that claim 3 is not anticipated by Sindhu et al.

Claim 4 recites that the shared memory includes a plurality of cell memories configured to store packet data and a pointer, where at least one of the cell memories is linked to another one of the cell memories via the pointer in the at least one cell memory. Sindhu et al. does not disclose or suggest the combination of features recited in claim 4.

The Examiner alleged that Sindhu et al. discloses these features and cited Figures 6 and 9, column 6, lines 24-67, and column 8, lines 33-65, of Sindhu et al. for support (Office Action, page 4). Applicants disagree.

Figure 6 and column 6, lines 24-67, of Sindhu et al. refer to an entry 600 in key buffer 516 of input switch 100. Entry 600 includes a key 602, full address 604, offsets 606, and an

indirect cell indicator 608. Nowhere does Sindhu et al. disclose that key buffer entry 600 stores packet data or a pointer, as would be required by claim 4.

Figure 9 and column 8, lines 33-65, of Sindhu et al. refer to reservation table 508 of input switch 100 (col. 8, lines 33-50). Sindhu et al. discloses that entries 906 in reservation table 508 store read request addresses (col. 8, line 66 - col. 9, line 5). Nowhere does Sindhu et al. disclose that entries 906 in reservation table 508 store packet data or a pointer, as would be required by claim 4.

For at least these additional reasons, Applicants submit that claim 4 is not anticipated by Sindhu et al.

Independent claim 26 recites a method for routing packets by a network device that includes a plurality of packet processors. The method comprises receiving a plurality of packets on at least one incoming packet stream; distributing the packets to the packet processors according to a load balancing scheme; processing, by the packet processors, the packets to determine routing information for the packets; and transmitting the processed packets on at least one outgoing packet stream based on the routing information.

Sindhu et al. does not disclose or suggest the combination of features recited in claim 26. For example, Sindhu et al. does not disclose or suggest a plurality of packet processors, as explained above with regard to claim 1. Therefore, Sindhu et al. cannot disclose or suggest distributing packets to the packet processors according to a load balancing scheme or processing, by the packet processors, the packets to determine routing information for the packets, for reasons similar to reasons given with regard to claims 1 and 2.

For at least these reasons, Applicants submit that claim 26 is not anticipated by Sindhu et al. Claims 27 and 28 depend from claim 26 and are, therefore, not anticipated by Sindhu et al. for at least the reasons given with regard to claim 26.

In paragraph III of the Office Action, the Examiner rejected claim 24 under 35 U.S.C. § 103(a) as allegedly unpatentable over Sindhu et al. Applicants respectfully traverse the rejection.

Claim 24 depends from claim 1. Without acquiescing in the Examiner's rejection with regard to claim 24, Applicants submit that claim 24 is patentable over Sindhu et al. for at least the reasons given with regard to claim 1.

In paragraph IV of the Office Action, the Examiner rejected claims 9 and 29 under 35 U.S.C. § 103(a) as allegedly unpatentable over Sindhu et al. in view of Sandquist. Applicants respectfully traverse the rejection.

Claims 9 and 29 depend from claims 1 and 26, respectively. Without acquiescing in the Examiner's rejection of claims 9 and 29, Applicants submit that the disclosure of Sandquist does not cure the deficiencies in the disclosure of Sindhu et al. identified above with regard to claims 1 and 26. Therefore, claims 9 and 29 are patentable over Sindhu et al. and Sandquist, whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 1 and 26.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of pending claims 1-82.

To the extent necessary, a petition for an extension of time under 35 C.F.R. 1.136

is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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